I Claim:

1. A circuit structure, comprising:

a silicon substrate having at least two etching trenches formed therein and defining a silicon block having sidewalls, said etching trenches etched out in a manner adjoining said sidewalls of said silicon block, said etching trenches disposed at angles with respect to one another prescribed by a form of said silicon block; and

layer structures disposed in said etching trenches, a function of the circuit structure resulting from an interaction of said layer structures disposed in said etching trenches.

2. The circuit structure according to claim 1, wherein said layer structures include conductive structures disposed in said etching trenches.

3. The circuit structure according to claim 2, further comprising field-effect transistors formed within said etching trenches and said silicon block, each of said field-effect transistors having a first diffusion region functioning as a first source/drain region and extending into said silicon block, a conductive gate region, and a second diffusion region functioning as a second source/drain region and extending into said silicon block, a conductive channel being formed between

said first and second source/drain regions in dependence on a potential of said conductive gate region.

4. The circuit structure according to claim 1, further comprising regions have at least one of different doping concentrations and different conductivity types are disposed within said silicon block.

5. The circuit structure according to claim 2,

wherein said etching trenches include a first etching trench and a second etching trench disposed adjacent to said first etching trench;

further comprising doped diffusion regions extending from said first and second etching trenches into said silicon block and have an overlap region; and

wherein said conductive structures within said first etching trench and said conductive structures within said second etching trench are electrically connected to one another by said first and second diffusion regions which extend from said first and second etching trenches into said silicon block.

6. The circuit structure according to claim 1, further comprising voltage supply lines and signal lines for said

layer structures are in each case accommodated in one of said etching trenches.

7. The circuit structure according to claim 6, wherein:

said etching trenches include a first etching trench and a second etching trench;

said voltage supply lines and said signal lines are in each case accommodated in said first etching trench;

said layer structures are accommodated in said second etching trench; and

said layer structures have interconnections accommodated in said second etching trench.

8. The circuit structure according to claim 1, wherein said silicon block is a silicon parallelepiped.

9. The circuit structure according to claim 8, wherein said etching trenches are four etching trenches disposed around said silicon parallelepiped.

10. The circuit structure according to claim 1, wherein the circuit structure is an SRAM memory cell.

11. The circuit structure according to claim 10, wherein the SRAM memory cell contains a plurality of field-effect transistors interconnected to form a flip-flop and a selection transistor.

12. The circuit structure according to claim 11, wherein:

said silicon block has a p-doped region and an n-doped region; and

said field-effect transistors interconnected to form said flip-flop contain both n-FETs and p-FETs, said n-FETs being disposed in a region of said p-doped region of said silicon block, and said p-FETs being disposed in a region of said n-doped region of said silicon block.

13. The circuit structure according to claim 11,

wherein said selection transistor has a source-drain path; and

further comprising a bit line disposed at a surface of said silicon substrate, said flip-flop connected to said bit line through said source-drain path of said selection transistor.

14. The circuit structure according to claim 11, further comprising a word line disposed in said etching trenches, said selection transistor being activated by said word line.

15. The circuit structure according to claim 14,

wherein said word line serves as a gate region of said selection transistor; and

further comprising a gate oxide layer disposed between said word line and said silicon block.

16. The circuit structure according to claim 13, wherein said silicon block has an upper region being a doped region and said bit line disposed at said surface of said silicon substrate being contact-connected to said upper region.

17. The circuit structure according to claim 16, wherein said upper region formed as said doped region serves as one of a source electrode and a drain electrode of said selection transistor.

18. The circuit structure according to claim 2, wherein said conductive structures disposed are formed from polysilicon.]

19. The circuit structure according to claim 2, wherein said layer structures are semiconductor layer structures.

20. An array configuration, comprising:

a multiplicity of circuit structures, including:

a silicon substrate having at least two etching trenches formed therein and defining silicon blocks having sidewalls, said etching trenches etched out in a manner adjoining said sidewalls of said silicon blocks, said etching trenches disposed at angles with respect to one another prescribed by a form of said silicon blocks; and

layer structures disposed in said etching trenches, a function of said circuit structures resulting from an interaction of said layer structures disposed in said etching trenches.

21. The array configuration according to claim 20,

wherein said etching trenches disposed in each case in a manner adjoining a specific sidewall of said silicon blocks are lengthened to form continuous etching trenches extending across a plurality of said silicon blocks; and

further comprising voltage supply lines and signal lines accommodated in said continuous etching trenches.

22. A method for fabricating an array configuration having a multiplicity of circuit structures, which comprises the steps of:

a) providing a silicon substrate;

b) etching first etching trenches in the silicon substrate in each case in a manner adjoining and defining first sidewalls of silicon blocks, the silicon blocks being formed from unetched parts of the silicon substrate;

c) filling the first etching trenches with a first protective insulation;

d) etching further etching trenches in each case in a manner adjoining and defining second sidewalls of the silicon blocks;

e) filling the further etching trenches with a second protective insulation; and

f) repeating steps d) and e) until all etching trenches have been produced.

23. The method according to claim 22, which further comprises:

selectively etching-out the first and second protective insulations; and

producing semiconductor layer structures in the etching trenches.

24. The method according to claim 22, which further comprises:

producing diffusion regions which extend into the silicon blocks by the steps of:

depositing one of an n-doped material and a p-doped material into respective etching trenches to a desired depth;

afterward, indiffusing one of the n-doped material and the p-doped material into the silicon blocks by a heat treatment step.

25. The method according to claim 22, which further comprises producing regions having at least one of different doping

concentrations and different conductivity types within the silicon blocks, from a surface of the silicon blocks, by an implantation process.

26. The method according to claim 22, which further comprises depositing conductive structures within the etching trenches.

27. The method according to claim 22, which further comprises forming field-effect transistors within the etching trenches and the block structures by the steps of:

producing a first diffusion region extending into a respective silicon block and functioning as a first source/drain region;

producing a conductive gate region disposed above the first diffusion region; and

producing a second diffusion region extending into the respective silicon block and functioning as a second source/drain region.

28. The method according to claim 22, which further comprises:

providing conductive structures within a first etching trench and within an adjacent second etching trench of the etching trenches; and

forming doped diffusion regions for electrically connecting the conductive structures, the doped diffusion regions being indiffused from the first and second etching trenches into the silicon blocks, such that they overlap within the silicon blocks.

29. The method according to claim 22, which further comprises forming the circuit structures as SRAM memory cells.

30. The method according to claim 29, which further comprises forming the SRAM memory cells with a plurality of field-effect transistors interconnected to form a flip-flop, and a selection transistor.

31. The method according to claim 26, which further comprises forming the conductive structures from polysilicon.

32. An SRAM memory cell, comprising:

a silicon substrate having a silicon block with regions having at least one of different doping concentrations and different conductivity types, said silicon substrate having at least two

etching trenches formed therein, said etching trenches in each case define a sidewall of said silicon block and embodied in a manner adjoining said sidewall, said etching trenches disposed at angles with respect to one another and prescribed by a form of said silicon block, said etching trenches together with said silicon block containing and defining circuit structures, said circuit structures including field-effect transistors, and voltage supply and signal lines, said field-effect transistors being embodied in a first etching trench of said etching trenches along said silicon block and containing a first diffusion region as a first source/drain region extending into said silicon block, a second diffusion region as a second source/drain region extending into said silicon block, and a gate region embodied in said first etching trench, said voltage supply and signal lines being embodied in a second etching trench of said etching trenches.

33. The SRAM memory cell according to claim 32, wherein further comprising conductive structures made of polysilicon disposed in said etching trenches.

34. The SRAM memory cell according to claim 33, further comprising doped diffusion regions extending into said silicon block and have an overlap region, said conductive structures in said first and second etching trenches are electrically connected to one another by said doped diffusion regions.

35. The SRAM memory cell according to claim 32, wherein:

said silicon substrate has a third etching trench formed therein; and

said field-effect transistors have interconnections embodied in said third etching trench.

36. The SRAM memory cell according to claim 32, wherein said silicon block is embodied as a silicon parallelepiped.

37. The SRAM memory cell according to claim 35, wherein said at least two etching trenches are two of four etching trenches formed in said silicon substrate and disposed around said silicon parallelepiped.

38. The SRAM memory cell according to claim 32, wherein:

said circuit structures include a selection transistor; and

said field-effect transistors are interconnected to form a flip-flop.

39. The SRAM memory cell according to claim 38, wherein:

said silicon block has an n-doped region and a p-doped region; and

said field-effect transistors interconnected to form said flip-flop contain both n-FETs and p-FETs, said n-FETs are disposed in a region of said p-doped region of said silicon block and said p-FETs are disposed in a region of said n-doped region of said silicon block.

40. The SRAM memory cell according to claim 38,

further comprising a bit line disposed at a surface of said silicon substrate; and

said selection transistor having a source-drain path connecting said field-effect transistors interconnected to form said flip-flop to said bit line.

41. The SRAM memory cell according to claim 38, further comprising a word line for activating said selection transistor, said word line disposed in one of said etching trenches.

42. The SRAM memory cell according to claim 41,

wherein said word line serves as a gate region of said selection transistor; and

further comprising a gate oxide layer disposed between said word line and said silicon block.

43. The SRAM memory cell according to claim 40, wherein said silicon block has a covering layer formed as a doped region with which said bit line disposed at said surface of said silicon substrate is contact-connected.

44. The SRAM memory cell according to claim 38, wherein said selection transistor has a source electrode and a drain electrode, one of said source electrode and said drain electrode of said selection transistor is formed in an upper region of the said silicon block.

45. An array configuration, comprising:

a silicon substrate having at least two etching trenches formed therein and defining silicon blocks having sidewalls, said etching trenches etched out in a manner adjoining said sidewalls of said silicon blocks, said etching trenches disposed at angles with respect to one another prescribed by a form of said silicon blocks; and

layer structures disposed in said etching trenches and forming a multiplicity of SRAM memory cells, a function of said SRAM memory cells resulting from an interaction of said layer structures disposed in said etching trenches.

46. The array configuration according to claim 45,

wherein said etching trenches disposed in each case in a manner adjoining a specific sidewall of said silicon blocks are lengthened to form continuous etching trenches extending across a plurality of said silicon blocks; and

further comprising voltage supply lines and signal lines accommodated in said continuous etching trenches.